REMARKS/ARGUMENTS

Claims 1-10 stand rejected in the outstanding Official Action. Claims 1 and 6 have been amended and newly written claim 11 offered for consideration. Therefore, claims 1-11 remain in this application.

The Examiner's indication of acceptability of Applicant's originally filed formal drawings is very much appreciated. Additionally, the Examiner's confirming Applicant's claim for priority and receipt of all certified copies of the priority documents is very much appreciated. Finally, the Examiner's consideration of prior art submitted in Applicant's previously filed Information Disclosure Statements is appreciated.

Claims 1-10 stand rejected under 35 USC §102 as being anticipated by Cooper (U.S. Patent 6,823,516). Applicant's claimed invention is a data processor which has the capability of not only changing from a first desired data processing performance level to a second desired data processing performance level, but also one which operates at an intermediate data processing performance level "during said change." Applicant has made minor modifications in independent claims 1 and 6 in order to clearly and positively recite structure which causes the data processor to operate at some intermediate level "during said change" from a first performance level to a second performance level. Newly written claim 11 has been added which recites the structure in "means plus function" language which is limited to the corresponding structures in the specification and equivalents thereof.

The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every

element of the claimed invention, arranged as in the claim." Thus, in order to support a rejection of Applicant's independent claims (and claims dependent thereon), it is incumbent upon the Examiner to demonstrate how or where the Cooper reference discloses each and every recited structure or method step and any recited interrelationships between said structures or method steps.

The Examiner suggests that the Cooper reference at column 5, lines 33-50 teaches a processor which temporarily operates at some intermediate data processing performance level "during said change." A review of this portion of Cooper, as well as other portions, will clarify that Cooper does not disclose operating at any intermediate processing level when making a change between two different performance levels.

Applicant agrees that, given that Cooper teaches "a plurality of high performance states" and that there is likely one performance state which is intermediate to other performance states, this disclosure alone does not anticipate or render obvious the subject matter of Applicant's invention. There is no suggestion that "during" the transition between two different performance requires or discloses that the Cooper device operates at some different intermediate performance level "during" that transition. Applicant's claim specifies "during said change" and therefore if Cooper fails to teach this operational interrelationship, it cannot anticipate or render obvious the subject matter of Applicant's claims.

The Examiner's attention is respectfully directed to Cooper at column 8, lines 6-13, where Cooper specifically discloses a problem in that "during" a change Cooper requires disabling of the processor during the latency of the transition between performance levels ("another software visible impact of a performance-state-enabled approach is that **transitions between**

performance states hold off CPU operation for the duration of time it takes to switch between the performance states." emphasis added, Column 8, lines 6-9). Cooper also recognizes that this "additional latency" in the operating system transition could, if long enough duration, "cause operating system failure." Thus Cooper clearly teaches an interruption in CPU operation during the transition between two levels of operation.

Thus, in view of the above, Cooper not operate at some intermediate processing level during the transition between two other different levels, and, instead, Cooper specifically teaches that one needs to "hold off CPU operations for the duration of time it takes to switch between the performance states." In other words, Cooper teaches away from any processor operation "during said change" and is the direct opposite of Applicant's claimed invention, i.e., continuing operation at an intermediate level for the duration of time it takes to switch between the performance states.

As a result of the above, not only does Cooper fail to disclose the subject matter of Applicant's independent claims 1 and 6, it specifically teaches that it is necessary to disable the CPU operation during transitions. Thus, while Cooper may have a plurality of different performance levels, one or more of which may be intermediate two of the performance levels, he specifically teaches that "during" the transition between any two levels, the CPU operation is disabled for some period of time. Applicant's claim, in contra-distinction thereto, positively recites that "during" the transition, the Applicant's device operates at an intermediate performance level during the transition. Quite clearly, Cooper does not anticipate nor can it render obvious the subject matter of Applicant's independent claims 1 and 6 and any further rejection of these claims or claims dependent thereon is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-11 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact Applicant's undersigned representative.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____
Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100